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March 9, 2004

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/763,306 01/23/04

Shih-Wei Chou et al.

METHOD TO IMPROVE PLANARITY OF ELECTROPLATED COPPER

## INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March | 6, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Sub 3/16/04

- U.S. Patent 6,346,479 to Woo et al., "Method of Manufacturing a Semiconductor Device having Copper Interconnects," discloses manufacturing high density semiconductor devices with submicron design features.
- U.S. Patent 6,207,222 to Chen et al., "Dual Damascene Metallization, " discloses multi-step plating to fill a Cu dual damascene opening.
- U.S. Patent 6,140,241 to Shue et al., "Multi-Step Electrochemical Copper Deposition Process with Improved Filling Capability, " describes a multi-step electrochemical method for forming a copper metallurgy on an integrated circuit which has high aspect ratio contact/via openings.
- U.S. Patent 6,136,707 to Cohen, "Seed Layers for Interconnects and Methods for Fabricating Such Seed Layers," discusses a method for making metallic interconnects.
- U.S. Patent 5,814,557 to Vankatraman et al., "Method of Forming an Interconnect Structure, " discloses an interconnect structure formed by filling a dual damascene structure with conductive material.

Sincerely,

Stephen B. Ackerman,

Reg. No. 37761

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